Field Programmable Gate Array Having Partitionable Embedded Memory
With Configurable Depth versus Width

ABSTRACT OF THE DISCLOSURE

A field programmable gate array (FPGA) has plural columns of run-time memory provided in each of one or more partitions. Each column of run-time memory has a plurality of configurable memory blocks (CMB's). Each CMB is programmably configurable at least into a shallow-and-widest mode where data words have a maximum bit width and into a deep-and-narrowest mode where data words have a minimum bit width. Each CMB spans plural interconnect buses and the bits of its widest data words are distributed among the spanned interconnect buses. When a deep-and-narrow mode is invoked, CMB's of alternate columns operate in complementary fashion so that bits of narrowed words from one CMB move through a first subset of the interconnect buses while bits of narrowed words from a second CMB, in an alternate column, move through a second subset of the interconnect buses, where the second subset is mutually exclusive of the first subset of the interconnect buses. On the other hand, when the shallow-and-widest mode is invoked, the bits of the wide words of CMB's in alternate columns shared interconnect buses on an overlapping basis. In one embodiment, the shared interconnect buses are tri-statable. Programmable joiners are provided for joining or disjoining the tri-statable interconnect buses of adjacent partitions.